AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) ~~An off-chip driver circuit having first to N^{th} off-chip drivers for using a data signal and first to N^{th} control signals respectively to determine whether to produce output signals according to corresponding control signals, being characterized in that:~~

~~at least one of the first to N^{th} off-chip drivers comprises a delay circuit(s) for outputting a signal having a given delay time compared with other signals of the remaining off-chip drivers.~~

An off-chip driver circuit, comprising;

a plurality of delay circuits, at least two of which have different delay times, in which the delay circuits receive a data signal and generate delayed data signals; respectively, and

a plurality of off-chip drivers for respectively receiving the delayed data signals from the respective delay circuits and generating respective output signals in response to respective control signals,

whrerein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals.

2. (Currently Amended) The off-chip driver circuit as claimed in claim 1, ~~wherein the delay circuit is added to an input terminal of the off-chip driver to delay the data signal.~~

wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.

3. (Currently Amended) ~~The off-chip driver circuit as claimed in claim 1, wherein the delay circuit is added to an output terminal of the off-chip driver to delay the output signals.~~

An off-chip driver circuit, comprising;

a plurality of off-chip drivers for respectively receiving a data signal and generating a plurality of output signals, respectively, in response to respective control signals; and

a plurality of delay circuits at least two of which have different delay times with respect to each other, in which the delay circuits respectively receive the output signals and generate delayed output signals, respectively,

whrerein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals.

4. (Currently Amended) The off-chip driver circuit as claimed in claim [[1]] 3, ~~wherein each of the off-chip drivers performs an NAND operation for a corresponding control signal and the data signal when a logical status of the inputted data signal is High, and an NOR operation for an inverse signal of a corresponding control signal and the data signal~~

~~when a logical status of the inputted data signal is Low. control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver is driven.~~

Wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.

5. (New) The off-chip driver circuit as claimed in claim 1, wherein a total drivability of the off-chip drivers is at least 80% of a target drivability.

6. (Currently Amended) A data output circuit, comprising:

~~first to Nth off-~~chip ~~drivers for outputting a data signal, respectively, in response to corresponding first to Nth control signals;~~

a plurality of delay circuits at least two of which have different delay times with respect to each other, in which the delay circuits receive a data signal and generate delayed data signals, respectively;

a plurality of off-chip drivers for respectively receiving the delayed data signals from the respective delay circuits and generating respective output signals in response to respective control signals;

a pre-driver circuit ~~for using~~ adapted to receive the data signal and drive ~~to drive~~ an output driver circuit; and

the output driver circuit connected to the outputs terminals of the off-chip drivers ~~circuit~~ and the pre-driver circuit,

wherein ~~at least one of the first to Nth off-chip drivers comprises a delay circuit for delaying the data signal.~~ the number of the off-chip drivers to be activated is changed from 0

to N in response to the respective control signals, and total drivability of the data output circuit depends on the number of the off-chip drivers to be operated according to the control signals.

7. (Currently Amended) The data output circuit as claimed in claim 6, wherein the pre-driver circuit receives the data signal and performs a ~~pulls up~~ pull-up or ~~pulls down~~ a pull-down function according to a logical status of the data signal.

8. (Currently Amended) The data output circuit as claimed in claim 6, ~~wherein each of the off-chip drivers performs an NAND operation for a corresponding control signal and the data signal when a logical status of the inputted data signal is High, and an NOR operation for an inverse signal of a corresponding control signal and the data signal when a logical status of the inputted data signal is Low.~~ wherein, when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.

9. (Currently Amended) The data output circuit as claimed in claim [[8]]6, wherein the output driver circuit comprises ~~each of the~~ output drivers ~~and off-chip drivers corresponding to the pre-driver circuit~~ connected to output terminals of the respective off-chip drivers and the pre driver circuit, wherein ~~if~~ when the control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver is driven.

10. (New) The data output circuit as claimed in claim 6, wherein a total drivability of the off-chip drivers is 80% of a target drivability and a drivability of the pre

driver circuit is 60% of the target drivability so that a drivability of the data output circuit varies from 60% of the target drivability to 140% of the target drivability.

11. (New) A data output circuit, comprising:

a plurality of off-chip drivers for respectively receiving a data signal and generating a plurality of output signals, respectively, in response to respective control signals;

a plurality of delay circuits at least of two of which have different delay times, in which the delay circuits respectively receive the output signals and generate delayed output signals, respectively,

a pre-driver circuit receiving the data signal and driving an output driver circuit; and

the output driver circuit connected to the output terminals of the delay circuits and the pre-driver circuit,

whrerein the number of the off-chip drivers to be activated is changed from 0 to N in response to the respective control signals, and a total drivability of the data output circuit depends on the number of the off-chip drivers to be operated according to the control signals.

12. (New) The data output circuit as claimed in claim 11, wherein the pre-driver circuit receives the data signal and performs a pull-up or a pull-down function according to the logical status of the data signal.

13. (New) The data output circuit as claimed in claim 11, wherein when operating at a logical status of the control signal being high, the off-chip drivers perform NAND operations, and when operating at a logical status of the control signal being low, the off-chip drivers perform NOR operations.

14. (New) The data output circuit as claimed in claim 11, wherein the output driver circuit comprises output drivers connected to output terminals of the delay circuits and the pre driver circuit respectively, wherein when the control signal of a given off-chip driver is at an enable level, the output driver connected to the given off-chip driver is driven.

15. (New) The data output circuit as claimed in claim 11, wherein a total drivability of the off-chip drivers is 80% of a target drivability and a drivability of the pre driver circuit is 60% of the target drivability so that a drivability of the data output circuit varies from 60% of the target drivability to 140% of the target drivability.